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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/787,290	06/28/2001	Jonathan Westphal	52254-016	6488

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ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.  
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE  
P.O. BOX 3791  
ORLANDO, FL 32802-3791

EXAMINER

THOMSON, WILLIAM D

ART UNIT	PAPER NUMBER
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2123

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<p align="center"><b>Office Action Summary</b></p>	Application No. 09/787,290	Applicant(s) WESTPHAL, JONATHAN	
	Examiner William Thomson Thomas H. Stevens	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 08 November 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

1. Claims 1-12 were examined.

### ***Response to Applicant's Arguments***

#### ***Abstract***

2. Applicant's are thanked for addressing this issue. Examiner recognizes amended abstract; however, is unclear as to the origin of the numerical notation (13b). Based on this finding, the objection stands.

#### ***Specification (References)***

3. Applicant's are thanked for addressing this issue. The reasoning behind the objection is since references are specific (i.e., citing pages relative to the written description) to the content of the invention, they are consider prior art regardless if the information is directly or indirectly related to the claims, otherwise one would question their purpose. Objection stands.

#### ***Specification (Footnotes)***

4. Applicant's are thanked for addressing this issue. Based on applicant's response and action, the objection is withdrawn.

***Claim Objections***

5. Applicant's are thanked for addressing this issue. Applicant, by admission, wasn't able to respond, therefore the objection stands.

***Claim Rejections - 35 USC § 102***

6. Applicant's are thanked for addressing this issue. Applicant's state the Turrini reference (U.S. Patent 5,886,902) does not represent the logic of a logic circuit as vector. The Turrini abstract contradicts the latter statement:: *In a computer implemented method, possible arrangements of items, such as components to be placed on semiconductor die are described in a permutation space expressed as a data structure stored in memory....A best ordering of items is determined in the vector space according to a predetermined criterion....* Additionally, applicants state the Turrini reference doesn't minimize or reduce the number of components, which is true; however, the claims the applicants mention in their response doesn't mention reduction verbatim.

Applicant's state prior art reference by Jain et al. (U.S. Patent 5,649,165), doesn't teach logic simplification.. Claim 31 of Jain et al., clearly states the following: A method using a computer-aided design system for logic design *verification using decision diagram **simplification**, the system comprising a first and a second separate digital circuit topology each comprising a set of primary outputs and a set of primary inputs both interconnected with logic gates, the logic gates being interconnected by*

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*wires, the topologies having a set of logical interdependencies associated with at least one of the logic gates in the system, the system further comprising a tentative cut selection region in one of the separate topologies and comprising a reflection tentative cut selection region in the other of the separate topologies...*

Based on the previous statements, the rejection stands.

***Final Office Action***

***Information Disclosure Statement***

7. The listing of references in the specification is not a proper information disclosure C.F.R. 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and M.P.E.P. j 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered. For example, on pages 14, 16, 17 and 26 the applicant refers to publications, however, since they have not been provided in a formal IDS, the examiner has not considered their relevance to the instant invention.
4. The information disclosure statements (IDS) submitted on March 15, 2001 and August 13, 2001 have been considered by the examiner. However, it is noted that they individually reference the same documents.

***Abstract***

8. The abstract is objected to regarding unknown numerical reference.

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9. The apparent attempts to incorporate subject matter into this application by reference to articles of Garrod and Borns, on page 14, Quine, 1952, and Quine, 1982 on pages 16 and 17, Digital Optics 1989, on page 26 and foot note to inventor's book on page 26 may be improper because they appear essential to the claimed invention, especially claim 4.

#### ***Specification***

10. The disclosure is objected to because of the following informalities: footnotes do not comport to standard U.S. practice. In general, matter that is the disclosure is not footnoted. Appropriate correction is required.

#### ***Claim Objections***

11. Claim 4 is objected to because of the following informalities: constructs of the claim does not comport with U.S. practices. The claims are replete with minor typographic errors, for example, the semicolon after the zero and the period in step f1 should be a comma, and semicolon respectively, and the period in step g1 should be a comma. Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 112***

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

13. Claim 4 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant

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regards as the invention. Specific examples follow: There is insufficient antecedent basis for the limitation of "then 6". The phrase "i.e." renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05 (d). The reference to the content of "figure 4" fails to point out what is included or excluded by claim language. The claim is an omnibus type claim. The claim is narrative in form and replete with indefinite and functional or operational language. The structure which goes to make up the device must be clearly and positively specified. The structure must be organized and corrected and correlated in such a manner as to present a complete operative device. The claim must be in one sentence form only. Note format of the claims in the patent cited.

### ***Claim Rejections - 35 USC § 102***

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

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Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

15. Claims 1-3, and 5-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Turrini and further rejected under 35 U.S.C. 102(b) as being anticipated by Jain et al. (165). Jain et al. (165) teaches a steps/means/apparatus/methods of representing the logic of a logical circuit to be designed as points and vectors in a vector space', using the points and vectors in the vector space to simplify the logic of the logic circuit to a simpler form; and designing/implementing the logical circuit using the simpler form are summarized in col. 8, lines 25-61, wherein the use of points and vector space to simplify the circuit (a BDD graph using points and vectors) is further described in col. 1, lines 16 to col. 15, line 27.

16. Turrini (902) teaches a steps/means/apparatus/methods of representing the logic of a logical circuit to be designed as points and vectors in a vector space; using the points and vectors in the vector space to simplify the logic of the logic circuit to a simpler form; and designing/implementing the logical circuit using the simpler form are summarized in the Abstract, figures 2, 3-6, 7-11c, col. 3, lines 35 et seq., and col. 4, lines 23 et seq.

17. Furthermore looking to processing elements inclusive of optical computers, digital computers, colorimetric computers, and analog computers are within the



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knowledge of ones of ordinary skill level prior to the applicant's invention for implementing these system at the time of their individual teachings and therefore Jain et al., and Turrini, individually, are anticipatory of the claim invention. These are merely platforms on which the Applicant's invention may run upon. A reference anticipates a claims if it discloses the claimed invention "such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention." See *In re Graves*, (CA FC) 36 USPQ2d 1697, *In re Grice*, 301 F.3d 929, 133 USPQ 365 (CCPA 1962) *Cohn v. United States Corse Co.*, 93 U.S. 366.

18. As to claim 4, because of the 1 12 20d rejections, the claim is so indefinite and incomplete, no art rejection is warranted as substantial guesswork would be involved in determining the scope and content of these claims. See *In re Steele*, 305 F.2d 859, 134 USPQ 292 (CCPA 19623,' *Ex par/e Brummer*, 12 USPQ 2d, page 1654,. and also *In re Wilson*, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970). Claim 4 stands rejected under 35 U S C 1 12 2nd paragraph. No ad rejection has been applied.

### **Conclusion**

19. The prior art made of record on the P.T.O. 892 has not been relied upon and is considered pertinent to applicant's disclosure. Careful consideration of the cited art is required prior to responding this Office Action, see 37 C.F.R. 1.111(c).

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**CONTACT INFORMATION**

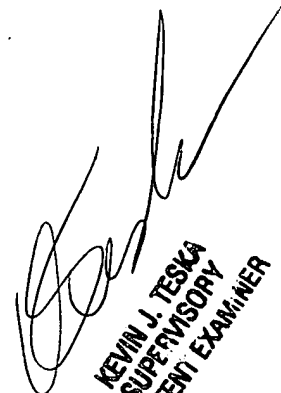
20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William D. Thomson whose telephone number is 703-305-0022. The examiner can normally be reached on 8:30-3:30 Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 17, 2005

WT



KEVIN J. TESKA  
SUPERVISORY  
PATENT EXAMINER